

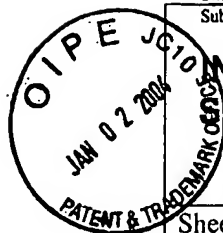
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| Application Number | 10/618,237 |
| Filing Date | July 11, 2003 |
| First Named Inventor | Gang Zhang et al. |
| Group Art Unit | 2825 |
| Examiner Name | Not Yet Assigned |
| Attorney Docket Number | 2879-030687 |

Sheet 1 of 3

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, cite and/or country where published. | T ² |
|--------------------|-----------------------|---|----------------|
| BP | 1 | R. HARJANI, R.A. RUTENBAR and L.R. CARLEY, "OASYS: A Framework For Analog Circuit Synthesis", IEEE Transactions On Computer-Aided Design, Vol. 8, No. 12, pp. 1247-1266, (December 1989). | |
| | 2 | M.G.R. DEGRAUWE, O. NYS, E. DIJKSTRA, J. RIJMENANTS, S. BITZ, B.L.A.G. GOFFART, E.A. VITTOZ, S. CSERVENY, C. MEIXENBERGER, G. VAN DER STAPPEN, and H. J. OGUEY, "IDAC: An Interactive Design Tool For Analog CMOS Circuits", IEEE Journal Of Solid State Circuits, Vol. Sc-22, No. 6, pp. 1106-1116, (December 1987). | |
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| | 4 | E. OCHOTTA, L.R. CARLEY and R.A. RUTENBAR, "Analog Circuit Synthesis For Large, Realistic Cells: Designing A Pipelined A/D Converter With ASTRX/OBLX", in Proc., IEEE Custom Integrated Circuit Conference, pp. 365-368, (1994). | |
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| | 6 | G.G.E. GIELEN and R.A. RUTENBAR, "Computer-Aided Design Of Analog And Mixed-Signal Integrated Circuits", Proceedings Of The IEEE, Vol. 88, No. 12, pp. 1825-1852 (December 2000). | |
| | 7 | J. RIJMENANTS, J.B. LITSIOS, T.R. SCHWARZ and M.G.R. DEGRAUWE, "ILAC: An Automated Layout Tool For Analog CMOS Circuits", IEEE Journal Of Solid State Circuits, Vol. 24, No. 2, pp. 417-425, (April 1989). | |
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| | 9 | U. CHOUDHURY and A. SANGIOVANNI-VICENTELLI, "Constraint Generation For Routing Analog Circuits", 27 th ACM/IEEE Design Automation Conference, pp. 561-566, (June 1990). | |
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| Examiner Signature | <i>Burden Bower</i> | Date Considered | 11/14/05 |
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|--------------------|-----------------------|---|----------------|
| BB | 11 | E. CHARBON, E. MALAVASI, D. PANDINI and A. SANGIOVANNI-VICENTELLI, "Imposing Tight Specifications On Analog IC's Through Simultaneous Placement And Module Optimization", IEEE 1994 Custom Integrated Circuits Conference, pp. 525-528, (May 1994). | |
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| | 13 | E. MALAVASI and A. SANGIOVANNI-VICENTELLI, "Area Routing For Analog Layout", IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 12, No. 8, pp. 1186-1197, (August 1993). | |
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| | 20 | S. MITRA, R.A. RUTENBAR, L.R. CARLEY and D. J. ALLSTOT, "Substrate-Aware Mixed-Signal Macro-Cell Placement In WRIGHT", IEEE Journal Of Solid-State Circuits, Vol. 30, No. 3, pp. 269-278, (March 1995). | |

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| Examiner Signature | <i>Burton Bower</i> | Date Considered | 11/14/05 |
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